REMARKS

1. Rejection of claims 1-9 under 35 U.S.C. 102(e) as being anticipated by Noritake et al. (US 6,410,358):

Claim 1 is amended to overcome this rejection. Specifically, the limitation of "**simultaneously** forming at least one thin film transistor and a plurality of **bumpy stacked structures** on the substrate, each of the bumpy stacked structures comprising a plurality of sub-stacked layers, which have at least two different widths" is added. These amendments are fully supported in the specification, such as in paragraph [0049], and in Figs. 10-14. No new matter is entered.

Regarding US 6,410,358, Noritake discloses a method of manufacturing a reflection type LCD (with reference to cols.1-2). The method includes:

Step 1 (Fig.3a): **forming a TFT structure** including a first gate electrode 11, a gate insulating film 12, an active layer 13, a channel 13c, a source 13s, a drain 13d, a stopper insulating film 14, an interlayer insulating film 15, contact holes 16, 17, a drain electrode 18, and a second gate electrode 19 on an insulating substrate 10;

Step 2 (Fig.3b): forming a first planarization insulating film 21 and a first resist film 22 over the layers formed in step 1, performing exposure and development processes using a first mask 23 having an opening positioned corresponding to the contact hole 17, and forming a contact hole 24 corresponding to the contact hole 17 by etching;

Step 3 (Fig.3c): forming a second planarization insulating film 25 and a second resist film 26, performing exposure and development processes using a second mask 32 having an opening positioned corresponding to a recess 29(27) to be formed, and **performing an etching process to form a concave 29(27)**;

Step 4 (Fig.3d): removing the second resist layer 26, and **forming a**

reflection display electrode 28 which contacts the source 13s so that the reflection display electrode 28 has concaves 29(27) in the display area.

Regarding US 6,410,358, Noritake discloses another method of manufacturing a reflection type LCD (with reference to cols.3-4). The method includes:

Step 1 (Fig.1a): **forming a TFT structure** including a first gate electrode 11 constituting a part of a gate signal line 51, a gate insulating film 12, an active layer 13, a channel 13c, a source 13s, a drain 13d, a stopper insulating film 14, an interlayer insulating film 15, contact holes 16, 17, a drain electrode 18 constituting a part of a drain signal line 52, and a second gate electrode 19 on an insulating substrate 10;

Step 2 (Fig.1b): forming a photosensitive resin film 70, and performing exposure and development processes using a first mask 71 having an opening positioned corresponding to a recess 27 to be formed;

Step 3 (Fig.1c): removing the first mask 71, forming a second mask 72 having an opening positioned corresponding to a contact hole 73, and performing exposure and development processes using the second mask 72 to from the contact hole 73;

Step 4 (Fig.1d): removing the second mask 72, developing the photosensitive resin film 70 to form a concave 74 and a contact hole 73, and forming a reflection display electrode 28 having a concave 74(27) and a contact hole 17.

Regarding US 6,410,358, Noritake discloses still another method of manufacturing a reflection type LCD (with reference to col.5 and Fig.4). The method illustrated in Fig.4 is similar to the method illustrated in Fig.1, only the sequence of step 2 and step 3 is swapped.

It can be seen from the above descriptions that in all three methods of forming a reflection type LCD, Noritake forms the TFT structure and

the concaves 29(27) separately. In other words, the concaves 29(27) are formed after the TFT structure is completely formed. In contrast, the method according to the present application forms the thin film transistor and the plurality of bumpy stacked structures **simultaneously**, and therefore requires **fewer photo masks** than Noritake's teaching does. As a result, the applicant believes that the method according to the present application cannot be anticipated by Noritake et al. as the examiner alleged.

In addition, the stacked structures according to the present application are **bumpy**, and each stacked structure has a plurality of sub-stacked layers having **at least two different widths**. On the other hand, Noritake's teaching forms a reflection display electrode 28 having **concaves 29(27) or 74(27)**, instead of a bumpy structure as the present application does. Since Noritake fails to teach or suggest the limitations "forming a plurality of **bumpy stacked structures**" and "each of the bumpy stacked structures comprising a plurality of sub-stacked layers, which have at least **two different widths**", the applicant contends that the amended claim 1 includes a novel and unobvious limitation over Noritake et al. (US 6,410,358).

Reconsideration of amended claim 1 is requested. Claims 2 and 3 are cancelled. Claims 5, 7, and 9 are amended in full accordance with the amended claim 1, and no new matter is entered. Claims 4-9 are dependent on claim 1 and should be allowable if claim 1 is allowed.

2. Rejection of claims 10-11 under 35 U.S.C. 103(a) as being unpatentable over Noritake et al. (US 6,410,358) in view of Yamazaki et al. (US 6,429,059):

With regard to US 6,429,059, Yamazaki discloses a method of producing semiconductor devices including the steps of forming

amorphous semiconductor film and N+ silicon layer. On the other hand, claims 10-11 of the present application respectively claim different materials of forming the sub-stacked layers of the bumpy stacked structures. These materials, such as an insulating layer, a gate electrode layer, an amorphous silicon layer, an N+ silicon layer, a metal layer, a common electrode, a source layer, a drain electrode, and a passivation layer, are all well known in the art, which the applicant does not deny. However, since claims 10-11 are dependent on claim 1, claims 10-11 therefore include the limitation "simultaneously forming at least one thin film transistor and a plurality of bumpy stacked structures". Yamazaki does not teach or suggest any steps of forming bumpy stacked structures, neither does Noritake. Thus, claims 10-11 are not obvious to Noritake et al. (US 6,410,358) in view of Yamazaki et al. (US 6,429,059).

Reconsideration of claims 10-11 is politely requested.

Sincerely,

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